



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,834	03/04/2004	Peer Gil Schmitt	003921.00148	3853
22907	7590	08/01/2005	EXAMINER	
BANNER & WITCOFF 1001 G STREET N W SUITE 1100 WASHINGTON, DC 20001			LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,834	SCHMITT, PEER GIL	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1 and 6-9 is/are rejected.
- 7) ☒ Claim(s) 2-5 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

1. Amendment filed on August 30, 1999 has been entered.
2. Claims 1-9 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Montoye (U.S. Patent No. 5,319,59).

Regarding claim 1, Montoye discloses a memory device (Figure 3) , comprising:
a plurality of addressable memory cells (Figure 3), each memory cell configured to store a first bit and a second bit (Column 2, lines 56-58), each memory cell including:
a first storage circuit (Figure 3, 301) configured to store the first bit; and
a second storage circuit (Figure 3, 302) configured to store the second bit and coupled to the first storage circuit (Figure 3), and further configured to deactivate the first storage circuit based on the second bit (Column 3, lines 29-67, Column 4, lines 1-34).

Regarding claim 6, Montoye discloses an apparatus (Figure 4), comprising:

a plurality of dual-bit memory cells (301, 302), each memory cell including:

a first storage circuit (301) configured to store a first bit, and a second storage circuit configured to store a second bit (Column 2, lines 56-60);

a first plurality of word lines (/ML) each controlling one of the first storage circuits (Figure 4); and

a second plurality of word lines (ML) each controlling one of the second storage circuits (Figure 4), wherein the first storage circuit includes a transistor (Figure 4, 304) having a gate, the gate coupled to the second storage circuit so as to receive a value of the second bit, and wherein the first storage circuit includes a flip flop (Figure 1, 101) that stores the first bit and that has a control node, the transistor further coupled between the control node and a fixed potential (Figure 4, 102), and wherein the second storage circuit includes a flip flop (302) that stores the second bit at a storage node, the gate of the transistor being coupled to the storage node (Figure 4), and further including a bit line pair (/BL, BL) each coupled to one of the memory cells, each bit line pair coupled to logic that combines the respective bit line pair into a single logical value (Column 3, lines 29-67, Column 4, lines 1-34).

Allowable Subject Matter

6. Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-5 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Montoye (U.S. Patent No. 5,319,590), and others, does not teach the claimed invention having an enable node and a first output node, wherein the first storage circuit has either a high or low impedance at the first output node depending upon a logical value of the enable node, the first bit line selectively receiving a logical value of the first output node.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LEI
PRIMARY EXAMINER